Thermal Management for Bare Die and Surface Mounted Packages

1. Introduction

Careful attention must be made to thermal characterization of components to ensure high product reliability. Higher level assembly of bare die in surface mount packages (SMT) adds complexity to proper thermal design. This in turn requires careful analysis of the bare die, package and PCB to ensure adequate thermal interfaces between bare die and package, package and PCB and finally PCB and heat sink. As device reliability is a strong function of its junction temperature and to ensure MTBF > 10^6 hours, junction temperatures for all transistors in a MMIC should be kept below maximum ratings, $T_{j\text{-max}}$, under all operating conditions. This application note defines important terms for thermal analysis, as well as methods for proper thermal design of the higher assemblies. General thermal concepts will first be described in section 2. Then, the details of an example will be discussed in section 3. PCB design recommendations for MMIC and SMT products will be provided in section 4. A glossary section is provided at the end.

2. Thermal Concepts Overview

DC bias and input signals inject power into chips. This power leaves the chip either in the form of output signals or heat. Heat is generated when electric current interacts with atoms in a material. This phenomenon is commonly referred to as Joule heating, ohmic heating, or resistive heating. Thermal considerations are in many ways analogous to electrical circuits. Whereas electrons carry electrical current, phonons carry heat current. A thermal equivalent of Ohm's law, V=IR, exists and is given as:

$$\Delta T = Q \cdot \Theta \qquad (1)$$

where

ΔT (in °C or K) = temperature difference or "potential" across two points in space,
Q (in W) = heat current flowing between the two points,
and Θ (°C/W or K/W) = thermal resistance between the two positions.

In Eqn. 1, ΔT is analogous to V, Q analogous to I, and Θ analogous to R. Package thermal characteristics may be summarized by Θ_{jc}, thermal resistance between transistor junction and case. Case is a point on the outside surface of the package. It is a function of materials used in the construction of the package as well as the die inside. Important parameters in calculating Θ_{jc} for a QFN are: the leadframe, mold compound, die attach epoxy, bare die material, bare die thickness, internal thermal vias, etc. For a QFN, Θ_{jc} refers to the outer die-paddle surface. In this document, bare die case will refer to back-side chip surface. Another common parameter is Θ_{ja}, which represents resistance between device junction to ambient environment. Θ_{ja} includes conductive, convective, and radiative heat paths. The effect of radiation is usually negligible. Another commonly used parameter is Θ_{ca} which represents resistance between the case and the ambient environment.

Thermal resistance for a given structure is calculated per Eqn. 2 below. For a material with thermal conductivity K, with length L, and cross-sectional area A, thermal resistance is

$$\Theta = L / (K \cdot A) \qquad (2)$$

where

L = length (in m)
K = thermal conductivity (in W/m-°C or W/m-K)
and A = cross-sectional area (in m^2)

For example, in Eqn. 2, area may be calculated as $A = \pi\ ^{2}$ for a filled via cylinder with radius, r. For a plated via, area may be calculated as $A = \pi (r_o^2 - r_i^2)$, which represents a hollow cylinder with outer radius r_o and inner radius r_i. In practice, the thermal power dissipates through a cone with a spreading angle□ which is a function of thermal conductivities of the adjacent materials.

$$\tan \square \sim \Theta_1 / \Theta_2 \qquad (3)$$

where Θ_1 and Θ_2 are thermal resistances for materials as illustrated in Figure 2 below.

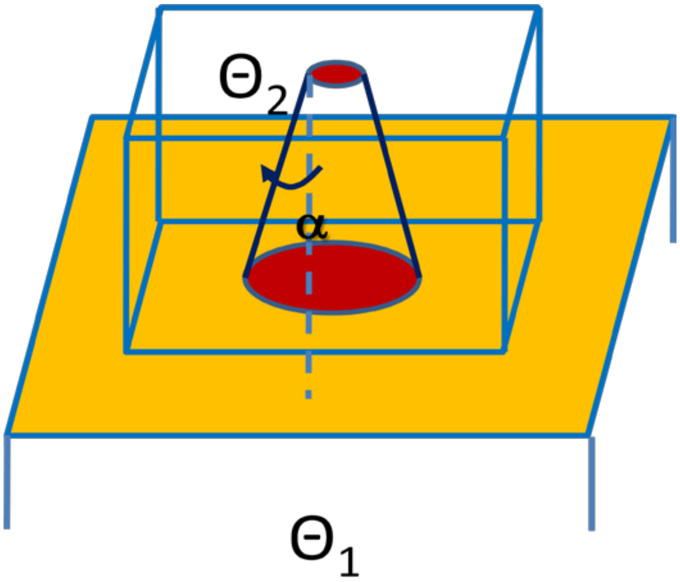

Figure 2. Spreading angle for thermal dissipation through a dissipation cone

In practice, GaAs thermal conductivity is much poorer than the copper leadframe for the QFN. The PCB underneath the QFN typically has poor thermal properties as well. Thermal conductivities for common materials are provided below in Table 1. Both metric and English units are provided for convenience.

Material	**Metric Units (W/m-°C or W/m-K)**
Aluminum (Al)	235
Copper (Cu)	394
Sn63 Solder	50
Gold (Au)	313
Diemat DM 6030Hk Epoxy	60
Ablestick 2600AT Epoxy	20
Alumina (Al_2O_3)	36 (99.8%)
Gallium Arsenide (GaAs)	55 @ 25 C
Sumitomo G770 Plastic Mold	0.88
Rogers 4350 (RO4350)	0.63
FR4	0.31

Table 1. Thermal conductivities for common materials

The thermal power dissipated by a transistor junction (P_{diss}) is calculated as

$$P_{diss} = P_{dc} - (P_{RF\_out} - P_{RF\_in}) \qquad (4)$$

Where P_{dc} is DC power consumption, P_{RF_in} is input RF power and P_{RF_out} is output power. Total dissipated power in a MMIC or QFN is the sum of all the thermal contributors. To accurately predict the thermal characteristics of a MMIC, accurate 3D thermal simulation must be performed taking into account nonlinear thermal material properties as well as coupling between thermal sources.

Junction temperature of a transistor can be estimated using

$$T_j = P_{diss} \times \Theta_{jc} + T_c \qquad (5)$$

Where Θ_{jc} is thermal resistance from junction to case, and T_c is the case temperature or the backside temperature of the chip. In calculating Θ_{jc}, spacing between transistor fingers, location of via, transistor geometry, metallization, etc. will have a noticeable impact.

Analogous with electric circuits, thermal resistances R1 and R2 in series add as

$$R_{total} = R1 + R2 \qquad (6)$$

Whereas thermal resistances in parallel are reduced as

$$R_{total} = 1 / [(1 / R1) + (1 / R2)]. \qquad (7)$$

Junction temperature of a device inside an SMT package mounted on a PCB can be calculated if thermal resistance values for the MMIC, package, and PCB, as well as the interface materials (epoxy, solder,…) are known. A thermal model for a QFN package on PCB is provided below in Figure 1 showing how to calculate junction temperature in a typical QFN assembly on PCB. The controlled heat sink temperature may be directly added to the calculated junction temperature or else ground in the model may be changed to the heatsink.

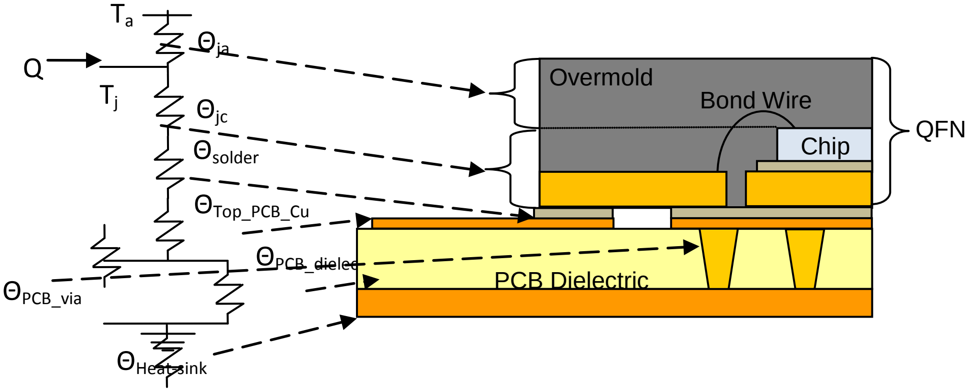

Fig. 1. Equivalent circuit model

For a QFN assembly on a PCB as shown in Fig. 1, Θ_{ja} is the thermal resistance from device junction to the top of plastic QFN package (ambient. Θ_{jc} is the sum of thermal resistances of GaAs, epoxy die attach, and leadframe. Effects of solder joint (Θ_{solder}), metal plating on PCB($\Theta_{Top\_PCB\_Cu}$), PCB (Θ_{PCB_Via} is much smaller than $\Theta_{PCB\_dielectric}$), and bottom plating metal ($\Theta_{Heat\text{-}sink}$) must also be considered.

To reduce the overall thermal resistance, each component needs to be optimized. A thinner GaAs substrate will have a better thermal conductivity. Thermal resistance of the epoxy die attach can also be reduced by using a thinner layer of a higher thermal conductivity epoxy such as Diemat DM 6030Hk. However, the epoxy should be thick enough to manage the different CTE between GaAs (5.7 ppm/°C) and Cu leadframe (16.5 ppm/°C). The epoxy attach process must be optimized for a void free layer. Epoxy thickness is typically controlled to between 0.5 to 1 mil (~ 10 to 50 µm). The Cu leadframe (typically 200µm thick) is a very good thermal conductor.

The solder used underneath the QFN package typically has a very good thermal conductivity (~ 30-50µm thick). However, careful attention must be made in patterning the solder to avoid a void free layer underneath the QFN.

The PCB material is a key contributor to the overall thermal characteristics of the assembly. Most of the thermal conduction will be through the via holes metallization. Therefore, the density of via holes and the fill-in material must be designed appropriately to reduce the overall thermal resistance. It is common to find via holes having a diameter 2x the substrate thickness, e.g. 16mil for a 8mil RO4003 PCB. The pitch between via holes is typically 5x the substrate thickness. Usually solder paste, Cu or other forms of conductors are used to fill via holes.

3. Example of a Junction Temperature Calculation

Endwave overmold QFN packages are built with 8 mil thick Cu leadframe and over molded with either a Hitachi or Sumitomo plastic compound. Photograph of an example 40 GHz Endwave QFN is provided below in Figure 3.

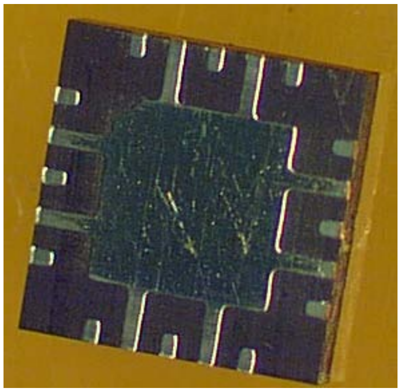

Figure 3 Bottom view of an Endwave QFN

A $3 \times 2\ mm^2$ 35-43GHz MMIC PA (EWP3801) with 1W output power, 16dB Gain biased at 6V, 850mA is packaged inside a 5x5 QFN. The output stage has 4x8x60 µm GaAs 0.15µm Phemt transistors that are biased at 6V, 220mA. The ground paddle for a 5x5 QFN is $3.6 \times 3.6\ mm^2$. QFN Leadframe is made of Cu and is 200µm thick. A 10µm Ablestick epoxy is used underneath the GaAs MMIC. An 8mil thick RO4003 PCB is used as the substrate. The via holes underneath the QFN are 400µm (inner diameter is 350µm) with a pitch of 1mm. Via holes are filled with Cu and solder paster. Maximum operating ambient temperature (T_A) is 85 °C.

Taking into account the GND paddle of $3.6 \times 3.6\ mm^2$ and diameter and pitch of via holes under the QFN, the # of via holes is calculated to be 16.

Worst-case power is dissipated when no RF power is applied to the chip. Since Θ_{ja} is much larger than Θ_{jc}, the thermal path to ambient is usually ignored. The total power dissipated in output stage is:

$$P_{diss} = 6 \times 0.22 = 1.32\ W \tag{8}$$

Using thermal simulation tools, the thermal resistance from junction to case Θ_{GaAs} is calculated to be 13.28°C/W.

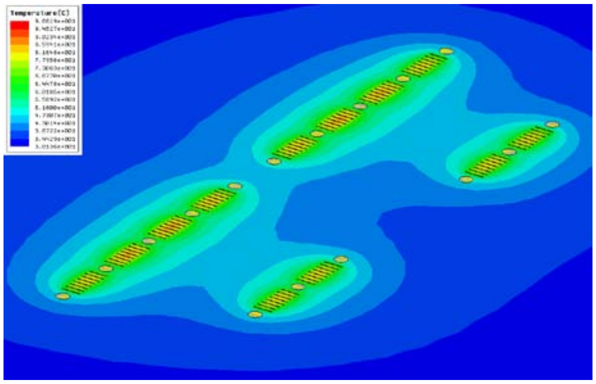

Figure 4. Thermal Simulation of a MMIC PA (last 2 stages)

The total thermal resistance for the remaining portions of the assembly is calculated as follows using Fig. 1 and equation (2).

Epoxy die attach: $\Theta_{epoxy} = (1/20)*10e^{-6}/(3e^{-3}*2e^{-3}) = 0.083\ °C/W$

20 is the thermal conductivity for the epoxy, 10 is the thickness of epoxy, and 3x2 is the area of the epoxy. A more accurate analysis will take into the account the spreading angle and the dissipation cone resulting in a smaller effective area for the thermal dissipation, thus a larger thermal resistance.

Leadframe: $\Theta_{leadframe} = (1/393)*200e^{-6}/(3.6e^{-3}*3.6e^{-3}) = 0.39\ °C/W$

$\Theta_{jc} = 13.28+0.083+0.39 = 13.753\ °C/W$

Solder_QFN: $\Theta_{solder} = (1/50)*20e^{-6}/(3.6e^{-3}*3.6e^{-3}) = 0.031\ °C/W$

PCB_Via_Cu: $A= 16*3.14*(0.2^{2}-0.175^{2})=0.452\ \text{mm}^{2}$
$\Theta_{\text{PCB\_Via\_Cu}} = (1/393)*200e^{-6}/0.452e^{-6}=1.126\ °\text{C/W}$

PCB_Via_Solder: $\Theta_{\text{PCB\_Via\_Solder}} = (1/50)*200e^{-6}/(16e^{-6}*3.14*0.175^{2})=2.6\ °\text{C/W}$

PCB_Via: $\Theta_{\text{PCB\_Via}} = \Theta_{\text{PCB\_Via\_Cu}}$ in parallel with $\Theta_{\text{PCB\_Via\_Solder}}$
$=(1.126*2.6)/(1.126+2.6)=0.786\ °\text{C/W}$

The thermal resistance of PCB dielectric is >> $\Theta_{\text{PCB\_Via}}$ and thus can be ignored. Note that filling the via with solder reduced its thermal resistance from 2.6 to 0.786°C/W.

Solder_PCB: $\Theta_{\text{jc}} = (1/50)*20e^{-6}/(3.6e^{-3}*3.6e^{-3})=0.031\ °\text{C/W}$

$\Theta_{\text{sum}}= 0.031+0.786+0.031+= 0.848\ °\text{C/W}$

$\Theta_{\text{total}}= 0.848 + 13.753 = 14.6\ °\text{C/W}$

$T_j= P_{\text{diss}} \times \Theta_{\text{total}} + T_A = 1.32 \times 14.6 + 85 =104.27\ °\text{C}$

The calculated T_j is much below the maximum junction temperature of 150 °C. Since MTBF is a strong function of T_j, a more detailed thermal simulation must be performed to take into account the coupling between transistors. Infrared microscopy can be used to verify the simulated results for T_j.

4. Printed Circuit Board Considerations

PCBs should be carefully designed for thermal characteristics when using high power chips and packages. Since high-frequency packages are especially sensitive to PCB design, Endwave provides recommended footprints for each package. A sample footprint is illustrated below in Figure 5. General guidelines will be discussed below for the designer to consider when deviations from recommended footprints are required.

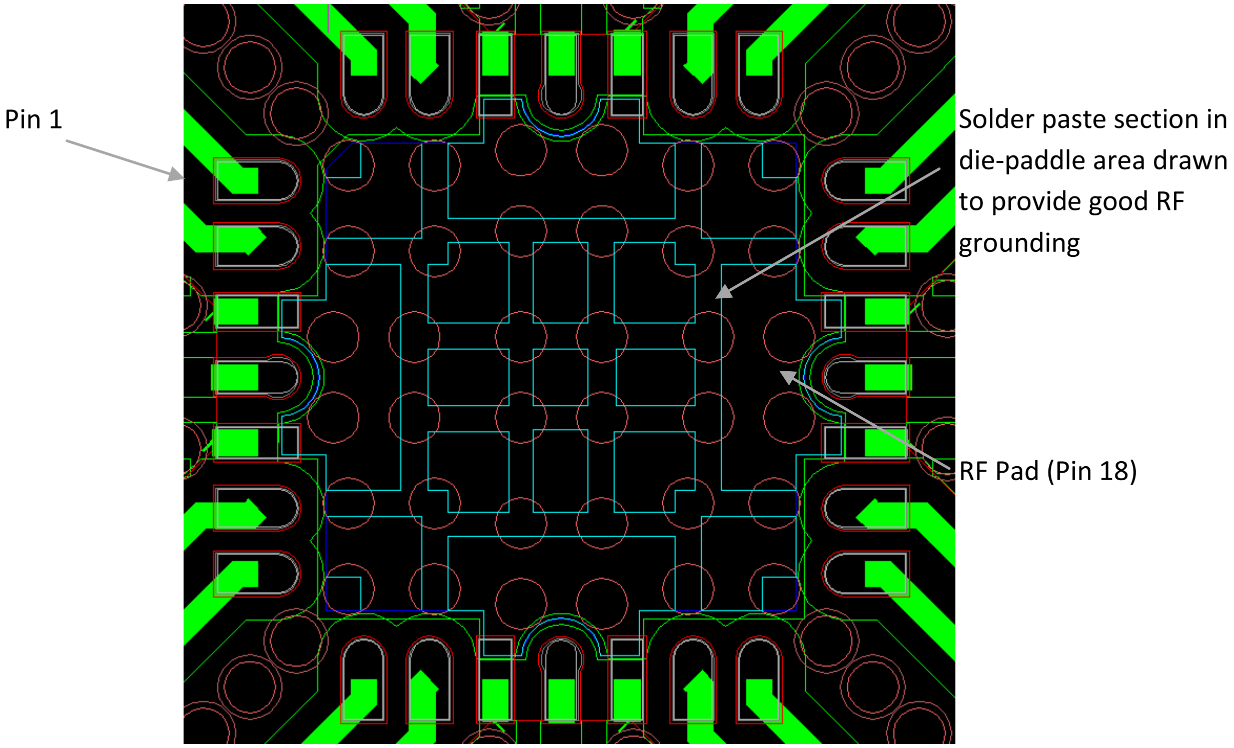

Figure 5 Sample PCB footprint for a 7x7/28L Endwave QFN

Dielectric Material Selection

The top layer PCB should be as thin as possible, i.e. 8 mils thick, to avoid needlessly increasing thermal resistance. Generally, thinner PCB materials may be desirable from electrical aspects at microwave frequencies.

Thermal Vias

PCBs should contain a maximal number of filled vias, rather than plated. This allows heat to be efficiently carried from the junction. Filled vias may result in a non-planar surface, which may result in increased solder stand-off. Consequences of increased solder stand-off include larger separation that may degrade both thermal and electrical characteristics. Instead, vias should be specified to be planar, which can be done with a PCB polishing process. Similarly, care should be taken with tenting, which can raise solder height and provide poor thermal interface.

When using bare die for a Chip-on-Board (CoB) assembly, care should be taken to avoid placing bond-pad locations over vias. Otherwise, chips may be exposed to a higher risk of cracking during the wirebond process. For Endwave QFNs, a set of vias need to be placed as close to the RF pads along the paddle edge in order to obtain the best electrical performance. Not doing so will results in additional ground inductance that degrade electrical performance.

Solder Paste and Solder Mask

In practice, die-paddle area solder paste will be required to be dispensed into several small sections. Note that in Figure 5 above, the turquoise solder paste areas are divided into several sections. Otherwise, a large solder section in the die-paddle area may cause QFN lifting, which increases total package stand-off height or even causes disconnects at pads, as illustrated in Figure 6 below. Additional concerns of large solder paste sections include out-gassing that may cause solder splatter and balling. Typical solder paste coverage is 50% to 75%. In order to provide excellent electrical grounding, solder-paste sections are created in the die-paddle area closest to the RF pad, as illustrated in Fig. 4. In that drawing, RF connections are available at center of each QFN, ie. pin 4, 11, 18, and 25. A total of 16 solder paste sections are applied in the example QFN. Solder stencils with thicknesses less than 2 mils are readily available and should be implemented for both thermal and electrical considerations. “No-clean” solder paste is recommended due to the low stand-off height.

Solder mask in the die-paddle area should be left open in order to accommodate solder paste. In the area of the QFN, solder mask should be applied around the pads in order to prevent shorting between contacts.

Figure 6 Illustration of solid solder paste pattern in die-paddle causing QFN lifting and open connections

Back-side Thermal Sinking

A back-side heat sink, as shown in above simulations, may be included to provide thermal cooling. Alternatively, additional laminate layers with thermal vias may suffice. As mentioned above, thermal vias should be filled with minimum voids. Further, advanced cooling methods may be applied including forced convection, active cooling, liquid-gas phase cooling, etc.

Glossary

ΔT – Temperature difference (°C or K)

Θ – A symbol representing thermal resistance in (°C/W or K/W)

Θja – Thermal resistance between transistor junction and top package surface that contact the ambient environment

Θjc – Thermal resistance between transistor junction and bottom package. In a QFN package, the case is the die-paddle surface. In a leaded package, the case is the bottom of the foot.

σ – A symbol sometimes used to represent thermal conductivity in lieu of K.

Die-paddle – grounded metal generally located centered in a QFN.

K - Abbreviation for thermal conductivity in units of (W/m-°C or W/m-K).

PCB – Printed Circuit Board

Q – Abbreviation for heat current in units of (W)

QFN – Quad Flat No-Lead Package

Solder mask – non-conductive polymer coating that serves to prevent solder bridging

Solder paste – solder powder suspended in flux that may be cured to create electrical connections

$T_{j\text{-max}}$ – Maximum channel temperature as defined to provide a lifetime of 10^6 hours (114 years). This parameter is foundry dependent and is individually provided on chip datasheets. pHEMT technology is typically specified to 150 °C, whereas HBTs are typically specified to 135 °C.

REFERENCES

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3. JESD51: Methodology for the Thermal Measurement of Component Packages, JEDEC website, http://www.jedec.org/DOWNLOAD/search/default2.cfm